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(71) Applicant : **PLESSEY SEMICONDUCTORS LIMITED**
Cheney Manor
Swindon, Wiltshire SN2 2QW (GB)

(72) Inventor : **Albon, Richard**
The Retreat,
Mary Tavy
Tavistock, Devon (GB)

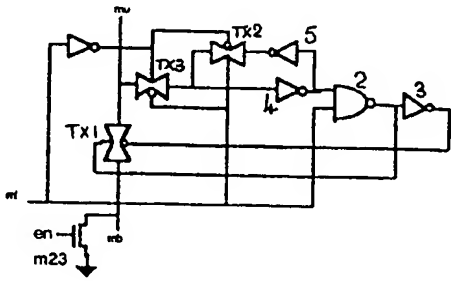
(74) Representative : **Hoste, Colin Francis**
The General Electric Company p.l.c.
GEC Patent Department
Waterhouse Lane
Chelmsford, Essex CM1 2QX (GB)

(54) Contents addressable memory.

(57) A contents addressable memory comprising an array of contents addressable memory cells arranged in rows and columns, each row of the array having a respective match line associated therewith for indicating a match if that be the case between address bit values of a data word or words to be retrieved from the memory and bit values held by the cells of the respective row, and a chain of cells associated one with each match line to indicate which, if there are more than one, of the match lines indicating a match is of the highest priority.

Figure 4

priority chain cell (pcc)



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The present invention relates to contents addressable memories. In particular although not exclusively the invention relates to contents addressable memories for use as fully associative cache memories.

In the past retrieval of data stored in random access memory (RAM) has been carried out for example by algorithmic searching under the control of a microprocessor from outside the memory. Since only a small part of the RAM address space could be accessed at any one time it was necessary to sequence through all addresses until a match was found.

Contents addressable memory (CAM), on the other hand, allows the contents of a comparand register to be compared directly with all addresses held in its address space on a row by row basis. In some applications, however, it is quite likely that multiple matches will occur in a contents addressable memory, and it becomes necessary to recover a recognisable address by taking the match having the highest priority, which priority may be ascribed, for example, on the basis of position in the memory array. This is where a priority coder becomes important, and in many cases there is a need to look at a large number of match lines and potentially a large number of matches. One such scheme has utilised a tree of OR and NAND gates to select match outputs from rows which are local to each other, the resulting outputs being gated through further stages to establish a final priority match with its address. In such a scheme having, say, 512 match lines there would need to be some five stages of logic distributed across the depth of the array. Some schemes use a chain of gates in cascade with buffering and look-ahead inserted at appropriate points along the chain to minimise delays, while others adopt a parallel approach with multi-input gates. The problem with such schemes is that they are limited to small CAM structures if they are to perform quickly and not take up too much chip area.

According to the present invention in a contents addressable memory comprising an array of memory cells arranged in rows and columns and means to apply address bit values to respective columns of said memory cells for comparison with bit values held by said cells, each row having a respective match line associated therewith for indicating a match or a mismatch between said applied address bit vlaues and the bit values held by said row, a priority encoder arrangement comprises a plurality of transmission gates associated one with each match line, said transmission gates being connected in a series path, with respective latch means to enable operation of each said transmission gate, and means to bias off in operation those transmission gates associated with match lines in respect of which a match is indicated.

Preferably said transmission gates are all initially biased on and said series path is arranged to be connected to a point of reference potential. The said latch means may be arranged to enable the operation of respective transmission gates in dependence upon the potential on said series path. There may be provided in respect of each of said transmission gates means responsive to a connection to said point of reference potential and to an indication of a match to detect the match occurring along said series path that is closest to said point of reference potential.

A contents addressable memory (CAM) in accordance with the present invention will now be described with reference to the accompanying drawings, of which:-

Figures 1 and 2 show diagrammatically two forms of contents addressable memory cell,

Figure 3 shows schematically a priority chain cell for a contents addressable memory,

Figure 4 shows diagrammatically a current sensing amplifier with a current to voltage converter, and

Figure 5 shows schematically a priority chain for a contents addressable memory.

Referring first to Figure 1, which shows a known form of contents addressable memory cell, bit values to be held in the cell are applied to a pair of cross-coupled inverters comprising transistors m1 to m4 from bit lines bl and blb by way of access transistors m5, m6 under the control of signals applied to a word line wl. The cells in the memory are arranged in rows and columns, and the bit values held in any row of cells represent address information in respect of data bits which are identified by that address information and which are held in a corresponding location in a random access memory (not shown).

In order to retrieve data bits held in the random access memory the necessary identifying address bit values are applied to the bit lines of respective columns of contents addressable memory cells in such a sense that at any cell where a match occurs between held bit values and address bit values the transistors of a pair m7, m9 and the transistors of a pair m8, m10. are arranged to be biased in opposite senses so that neither pair offers a conductive path between a match line ml and ground. At all cells where a mis-match occurs, however, the transistors of one or other pair m7, m9 or m8, m10 are arranged to be biased in the sense to provide a conductive path from the match line ml to ground.

The match lines ml or a row of memory cells are connected in series, and before a retrieval cycle the match lines of all rows are arranged to be charged to vdd. On any row where one or more mis-matches occur the match line is drawn down to ground potential, whereas on a row where all the held bit values match the identifying address bit values which have been applied to the bit lines, the potential of the row match line remains at vdd, indicating a match on that match line.

In an alternative form of memory cell shown in

Figure 2, which forms part of the subject matter of co-pending UK Patent Application No. 9308778.1, when a match occurs at any cell transistors m24 and m25 in that cell are arranged to be biased by the respective bit values to as to apply to the node nl a forward bias for a transistor m26 which is connected in series in the match line between mi and mo. When a complete match occurs along a row, therefore, the match line transistors 26 of the cells in that row offer a conductive path along the row which may be sensed by means of a current sensing circuit such as that shown in Figure 3.

Referring now to the current sensing circuit shown in Figure 3, in dependence upon the value of a current flowing in operation into a terminal mb from an associated match line ml and the value of a current flowing into a terminal mu from a dummy load (not shown), which currents are passed by a current transfer circuit m10 to m13 to respective current mirrors m14, m16 and m15, m17, a current to voltage converter comprising a single-ended current mirror m18, m19 provides a voltage output indicating which current is the larger. Thus if the associated match line is conducting, indicating a complete match along the respective row of memory cells, the value of current flowing into the terminal mb is arranged to be larger than the value of current from the dummy load, whereas in the event of a mis-match along the respective row substantially no current flows into the terminal mb.

Referring now to Figures 4 and 5, an arrangement in accordance with the present invention for determining, in the event of a plurality of match lines indicating a match along the respective rows, which of the matches has the highest priority, comprises a chain of priority chain cells, one of which is shown schematically in Figure 4, each connected to receive signals from a respective one of the match lines of the array of memory cells. Each priority chain cell 1 comprises a transmission gate TX1, which in its simplest form may comprise a pair of transistors (not shown) of opposite conductivity type having their major current paths connected in parallel. The conductive state of the transmission gate TX1 is arranged to be controlled by signals from the respective match line ml by way of a NAND gate 2 and an inverter 3. The NAND gate 2 has its second input connected to a latch circuit comprising inverters 4 and 5 and a second transmission gate TX2.

In operation all the nodes of the chain between the respective transmission gates TX1 are first drawn down to ground potential by way of transistors m23 (Figure 4) which are then turned off, leaving one connection to ground by way of a transistor m20 at the top of the chain. At this time the NAND gate 2 is enabled by way of a third transmission gate TX3 and inverter 4, which applies a potential approaching vdd to the second input of the NAND gate 2.

In the subsequent comparison cycle any match lines ml on which a match is indicated are arranged to apply a potential approaching vdd to the input of the respective priority chain cell, whereupon the respective transmission gate TX1 is biased off by way of the respective NAND gate 2 and inverter 3. As indicated in Figure 5 respective current sensing circuits 6, each of the form shown in Figure 3, are then used to detect the interruption in the current path down the chain. It will be appreciated that only in the case of the highest prioity chain cell 1 in the chain in which the resepctive transmission gate TX1 is biased off will a current path to ground still be available at the terminal mu of the respective current sensing circuit 6, the current paths to ground in respect of all inputs mu connected lower in the chain being blocked by the gate or gates TX1 that have been biased off. A path to ground is offered to all the mb inputs, of approximately double the impedance of the chain of gates TX1, by way of a transistor m21. In this use of the circuit of Figure 3 the current transfer circuits comprising transistors m10 to m13 are controlled by the signals from the respective match line circuits, only those in respect of rows in which a complete match occurs being switched so as to operate the respective current to voltage converters. The output from the circuit 6 in respect of the match highest up the chain will therefore be of the opposite sense to those of any other matches down the chain, indicating the match of highest priority, while all other circuits 6 will be disabled.

Claims

1. A contents addressable memory comprising an array of memory cells arranged in rows and columns and means to apply address bit values to respective columns of said memory cells for comparison with bit values held by said cells, each row having a respective match line associated therewith for indicating a match or a mis-match between said applied address bit values and the bit values held by said row, wherein a priority encoder arrangement comprises a plurality of transmission gates associated one with each match line, said transmission gates being connected in a series path, with respective latch means to enable operation of each said transmission gate, and means to bias off in operation those transmission gates associated with match lines in respect of which a match is indicated.

2. A contents addressable memory in accordance with Claim 1 wherein said transmission gates are initially all biased on and said series path is arranged to be connected to a point of reference potential.

3. A contents addressable memory in accordance with Claim 2 wherein said latch means is arranged to enable operation of the respective transmission gates in dependence upon the potential on said series path.

4. A contents addressable memory in accordance with Claim 1 wherein there are provided in respect of each of said transmission gates means responsive to a connection to said point of reference potential and to an indication of a match to detect the match occuring along said series path that is closest to said point of reference potential.

Figure 1

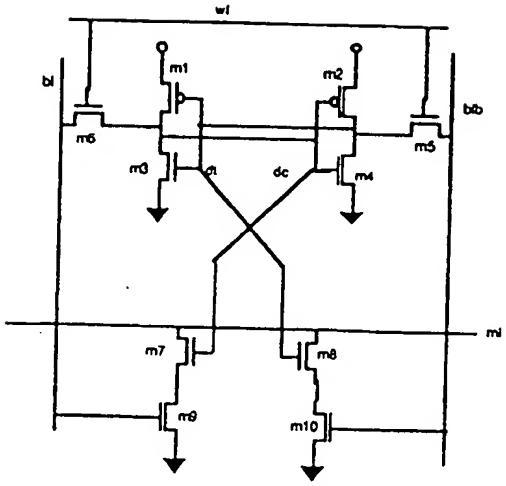


Figure 2

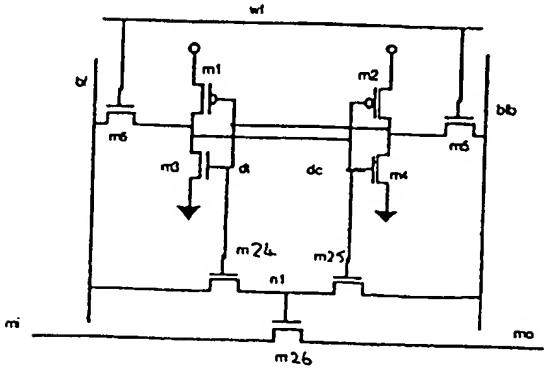


Figure 3

current sense amplifier (csa)
with I to v converter

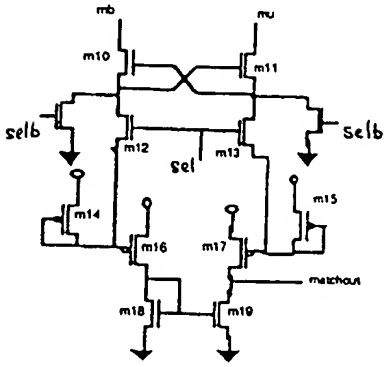


Figure 4

priority chain cell (pcc)

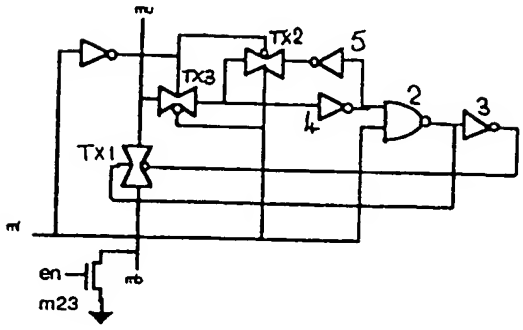
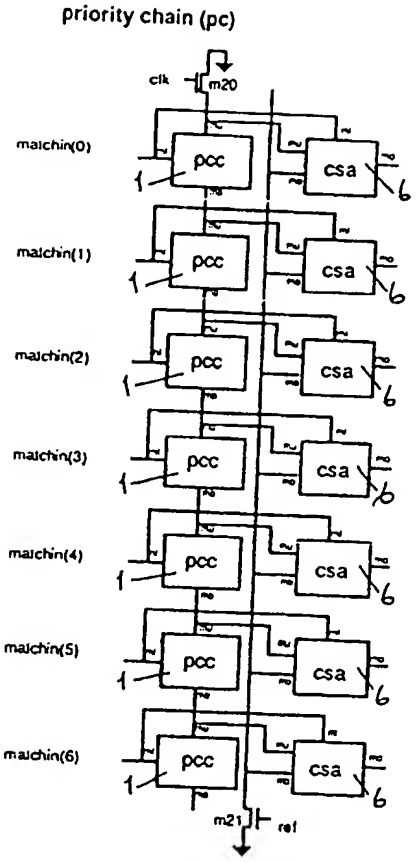


Figure 5


priority chain (pc)
clk
m20
matchin(0)
matchin(1)
matchin(2)
matchin(3)
matchin(4)
matchin(5)
matchin(6)
pcc
csa
m21
ref

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 94 30 2962

DOCUMENTS CONSIDERED TO BE RELEVANT

	Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
1	A	US-A-4 831 586 (NAKAGAWA ET AL.) * abstract * * column 4, line 48 - column 6, line 58; figures 1,3 *	1	G11C15/00
1	A	IEEE JOURNAL OF SOLID-STATE CIRCUITS. vol. 24, no. 4 , August 1989 , NEW YORK US pages 1003 - 1013 WADE ET AL. 'A TERNARY CONTENT ADDRESSABLE SEARCH ENGINE' * page 1008, line 43 - page 1011, line 10; figures 5-9 *	1	

TECHNICAL FIELDS SEARCHED (Int.Cl.5)
G11C

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	27 June 1994	Stecchina, A

CATEGORY OF CITED DOCUMENTS
X : particularly relevant if taken alone
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